

2812



Modified 02-03

 PTO/SB/21 (01-03)
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 Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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TRANSMITTAL FORM <small>(to be used for all correspondence after initial filing)</small>	Application / Conf. No.	10/092,051 / 7802
	Filing Date	March 04, 2002
	First Named Inventor	Stephen M. Douglass
	Examiner Name	Stacy Whitmore
	Art Unit	2812
Express Mail Receipt No.	Patent No.	
Total Number of Pages in This Submission	Attorney Docket Number	X-923 US

ENCLOSURES (check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Amendment / Reply <input type="checkbox"/> Preliminary Amendment <input type="checkbox"/> After Final <input type="checkbox"/> Affidavit(s)/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Change Status to LARGE ENTITY <input type="checkbox"/> Express Abandonment Request <input checked="" type="checkbox"/> Information Disclosure Statement (Supplemental) <input checked="" type="checkbox"/> Substitute PTO-1449(s) IDS by Applicant (PTO/SB/08A) <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Assignment Papers (with Recordation Cover Sheet) <input type="checkbox"/> Declaration / Oath <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition - <input type="checkbox"/> To Convert a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund	<input type="checkbox"/> After Allowance Communication to <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Return Receipt Postcard <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): <div style="border: 1px solid black; padding: 5px; margin-top: 5px;"> One Copy Each of the Ninety-Eight(98) References Cited </div>
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Customer Number	<div style="border: 1px solid black; padding: 5px; display: inline-block;"> 24309 <small>(Customer Number)</small> </div>	Reg. Number 51,959
Attn:	Justin Liu	
Signature		
Date	December 12, 2003	Charge any additional fees required/credit any overpayment to our Deposit Account Number: 24-0040

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Typed or Printed Name	Julie Matthews		
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This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.



X-923 US

PATENT

IN THE UNITED STATES PATENT OFFICE

Applicants: Stephen M. Douglass
Assignee: Xilinx, Inc.
Title: "Method of Designing Integrated Circuit Having
Both Configurable and Fixed Logic Circuitry"

Serial No.: 10/092,051 File Date: March 4, 2002
Examiner: Stacy Whitmore Art Unit: 2812
Docket No.: X-923 US Conf. No.: 7802

COMMISSIONER FOR PATENTS
P.O. BOX 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant brings to the attention of the Examiner the Ninety-Eight (98) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

The enclosed references are being cited after the receipt of a first office action but prior to any final action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein, is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,

Justin Liu
Attorney for Applicant
Reg. No. 51,959

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Julie Matthews
Name

Signature

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PTO/SB/08A (10-01)

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	7
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Complete if Known

Applicati n / C nf. No.	10/092,051 / 7802
Filing Dat	March 04, 2002
First Named Invent r	Stephen M. Douglass
Art Unit	2812
Examiner Name	Stacy Whitmore
Attorney Docket Number	X-923 US

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 4,758,985	07-19-88	Carter	
		US- 5,142,625	08-25-92	Nakai	
		US- 4,855,669	08-08-89	Mahoney	
		US- 34,363	08-31-93	Freeman	
		US- 5,072,418	12-10-91	Boutaud et al.	
		US- 5,274,570	12-28-93	Izumi et al.	
		US- 5,550,782	08-27-96	Cliff et al.	
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		US- 5,504,738	04-02-96	Sambamurthy et al.	
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		US- 6,578,174	06-10-03	Zizzo	
		US- 6,483,342	11-19-02	Britton et al.	
		US- 5,740,404	04-14-98	Baji	
		US- 5,581,745	12-03-96	Muraoka	
		US- 5,742,179	04-21-98	Sasaki	
		US- 5,600,845	02-04-97	Gilson	
		US- 5,574,930	11-12-96	Halverson Jr., et al.	

FOREIGN PATENT DOCUMENTS

[illegible]

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		Filing Date	March 04, 2002		
		First Named Inventor	Stephen M. Douglass		
		Art Unit	2812		
		Examiner Name	Stacy Whitmore		
Sheet	2	of	7	Attorney Docket Number	X-923 US

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		Christian Iseli et al., "SPYDER: A RECONFIGURABLE VLIW PROCESSOR USING FPGA's," IEEE, July 1993, pp. 17-24, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		MICHAEL I. WIRTHLIN et al., "THE NANO PROCESSOR: A LOW RESOURCE RECONFIGURABLE PROCESSOR," IEEE, February 1994, pp. 23-30, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		ANDRE' DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

Examiner Signature		Date Considered	
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¹ Applicant's unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached..

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	3	of	7
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Complete if Known

Applicati n / C nf. N .	10/092,051	/	7802
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Filing Date	March 04, 2002
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First Named Inventor	Stephen M. Douglass
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Art Unit	2812
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Examiner Name	Stacy Whitmore
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Attorney Docket Number	X-923 US
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U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 5,473,267	12-05-95	Stansfield	
		US- 5,742,180	04-21-98	DeHon et al.	
		US- 5,737,631	04-07-98	Trimberger	
		US- 5,748,979	05-05-98	Trimberger	
		US- 10/043,769	01-09-02	Schulz	
		US- 6,026,481	02-15-00	New et al.	
		US- 5,705,938	01-06-98	Kean	
		US- 5,500,943	03-19-96	Ho et al.	
		US- 10/001,871	11-19-01	Douglass et al.	
		US- 5,809,517	09-15-98	Shimura	
		US- 5,543,640	08-06-96	Sutherland et al.	
		US- 5,574,942	11-12-96	Colwell et al.	
		US- 6,604,228	08-05-03	Patel et al.	
		US- 5,933,023	08-03-99	Young	
		US- 09/991,412	11-16-01	Herron et al.	
		US- 6,389,558	05-14-02	Herrmann et al.	
		US- 5,732,250	03-24-98	Bates et al.	
		US- 5,889,788	03-30-99	Pressly et al.	
		US- 5,874,834	02-23-99	New	
		US- 5,835,405	11-10-98	Tsui et al.	

FOREIGN PATENT DOCUMENTS

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		Applicant / Conf. No.	10/092,051 / 7802
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Date	March 04, 2002
		First Named Inventor	Stephen M. Douglass
		Art Unit	2812
		Examiner Name	Stacy Whitmore
		Attorney Docket Number	X-923 US
Sheet	4	of	7

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-107 to 2-108, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		<u>CHRISTIAN ISELI et al.</u> , "AC++ COMPILER FOR FPGA CUSTOM EXECUTION UNITS SYNTHESIS," 1995, pp. 173-179, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		<u>INTERNATIONAL BUSINESS MACHINES</u> , "POWERPC 405 EMBEDDED PROCESSOR CORE USER MANUAL," 1996, 5TH Ed., pp. 1-1 TO X-16, International Business Machines, 1580 Rout 52, Bldg. 504, Hopewell Junction, NY 12533-6531.	
		<u>YAMIN LI et al.</u> , "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
		<u>INTERNATIONAL BUSINESS MACHINES</u> , "PROCESSOR LOCAL BUS" Architecture Specifications, 32-Bit Implementation, April 2000, First Edition, V2.9, pp. 1-76, IBM Corporation, Department H83A, P.O. Box 12195, Research Triangle Park, NC 27709	
		<u>XILINX, INC.</u> , "VIRTEX II PLATFORM FPGA HANDBOOK, December 6, 2000, v1.1, pp 33-75, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	

Examiner Signature	Date Considered
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Sheet	5	of	7
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		Number - Kind Code (if known)			
		US- 6,011,407	01-04-00	New	
		US- 6,172,990	01-09-01	Deb et al.	
		US- 09/991,410	11-16-01	Herron et al.	
		US- 5,760,607	06-02-98	Leeds et al.	
		US- 5,892,961	04-06-99	Trimberger	
		US- 2003/0062922	04-03-03	Douglass et al.	
		US- 09/917,304	07-27-01	Douglass et al.	
		US- 6,601,227	07-29-03	Trimberger	
		US- 09/861,112	05-18-01	Dao et al.	
		US- 09/858,732	05-15-01	Schulz	
		US- 2001/0049813	12-06-01	Chan et al.	
		US- 5,914,902	06-22-99	Lawrence et al.	
		US- 6,541,991	04-01-03	Horncheck et al.	
		US- 6,154,051	11-28-00	Nguyen et al.	
		US- 6,181,163	01-30-01	Agrawal et al.	
		US- 6,356,987	03-12-02	Aulas	
		US- 6,532,572	03-11-03	Tetelbaum	
		US- 6,211,697	04-03-01	Lien et al.	
		US- 6,163,166	12-19-00	Bielby et al.	
		US- 6,272,451	08-07-01	Mason et al.	

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Date Considered

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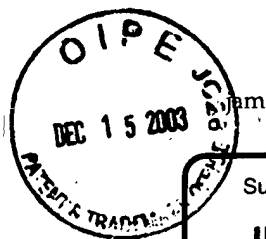
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Sheet 7 of 7

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		US- 6,522,167	02-18-03	Ansari et al.	
		US- 6,434,735	08-13-02	Watkins	
		US- 6,588,006	07-01-03	Watkins	
		US- 6,539,508	03-25-03	Patrie et al.	
		US- 6,587,995	07-01-03	Duboc et al.	
		US- 6,242,945	06-05-01	New	
		US- 6,460,172	10-01-02	Insenser Farre et al.	
		US- 6,353,331	03-05-02	Shimanek	
		US- 6,507,942	01-14-03	Calderone et al.	
		US- 6,518,787	02-11-03	Allegrucci et al.	
		US- 6,611,951	08-26-03	Tetelbaum et al.	
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